UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/745,370	12/22/2000	George Beshara Bendak	AMCC4460	8834

7590 09/08/2004

Terrance A. Meador
INCAPLAW
1050 Rosecrans Street
Suite K
San Diego, CA 92106

EXAMINER	
ODLAND, DAVID E	
ART UNIT	**PAPER NUMBER**
2662	

DATE MAILED: 09/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/745,370	Applicant(s) BENDAK ET AL.	
	Examiner David Odland	Art Unit 2662	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-46 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-46 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 4.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 18 and 25 objected to because of the following informalities: both of these claims have minor grammatical errors. Claim 18 recites "...in response the hierarchical..." in line 1. Claims 25 recites "...in response the hierarchical..." in line 5. In both claims, the term –to- should be inserted between "response" and "the". Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-18, 20,21 are rejected under 35 U.S.C. 102(b) as being anticipated by Ayanoglu (USPN 5,717,689), hereafter referred to as Ayanoglu.

Referring to claim 1-18, 20, 21 Ayanoglu discloses a method for segmenting a digital frame structure, the method comprising defining a hierarchical order in the overhead section of digital frame structure communications (values of the FEC are defined for an ATM cell (see abstract and column 2 lines 16-30)), and processing communications in response to the hierarchical order of overhead section bytes (the FEC is processed at the receiving end of the ATM cell (see figures 1-3));

wherein processing communications in response to the hierarchical order of overhead section bytes includes processes selected from the group including synchronization, scrambling,

forward error correction, and node segmented channel communication (the FEC is defined for the cell (see abstract and column 2 lines 16-30));

wherein defining a hierarchical order in the overhead section of digital frame structure communications includes defining a frame overhead section in response to characteristics selected from the group including the quantity of overhead bytes, the location of overhead bytes, and the value of overhead bytes (the value of the FEC is chosen (see abstract, column 1 lines 16-30 and column 20 lines 41-57));

defining a hierarchical order in the overhead section of digital frame structure communications includes defining a frame overhead section with a plurality of byte locations (a particular section of bytes makes up the overhead of a cell (see items 280 and 256 in figure 25)) and the method further comprising selecting overhead byte locations from the plurality of byte locations (certain overhead bytes are used for addressing and some are used for FEC calculations (see figures 23-26)) and wherein processing communications in response to the hierarchical order of overhead section bytes in a hierarchical order includes processing in response to the selected overhead byte locations (the FEC is processed (see abstract, column 1 lines 16-30 and column 20 lines 41-57));

wherein defining a hierarchical order in the overhead section of digital frame structure communications includes defining an overhead section with a plurality of overhead byte quantities (the ATM header comprises a number of bytes (see figure 25)) and the method further comprising selecting a quantity of overhead bytes from the plurality of overhead byte quantities (see abstract, column 1 lines 16-30 and column 20 lines 41-57)) and wherein processing communications in response to the hierarchical order of overhead section bytes includes

processing in response the selected quantity of overhead bytes (the FEC is performed (see abstract, column 1 lines 16-30 and column 20 lines 41-57));

selecting overhead byte values from the plurality of overhead byte values and wherein processing communications in response to the overhead section bytes in a hierarchical order includes processing in response the selected overhead byte values (the FEC value and field size changes over time thus it has multiple possible values and particular chosen values are processed (see abstract, column 1 lines 16-30 and column 20 lines 41-57));

wherein defining a hierarchical order in the overhead section of digital frame structure communications includes defining an overhead section with a first configuration of overhead bytes and a second configuration of overhead bytes (the FEC value and field size changes over time thus it has multiple configurations (see abstract, column 1 lines 16-30 and column 20 lines 41-57)) and wherein processing communications in response to the hierarchical order of overhead section bytes includes processing communications in a first process in response to the first configuration of overhead bytes and processing communications in a second process in response to the second configuration of overhead bytes (the multiple configurations of the FEC are processed be receiving stations (see abstract, column 1 lines 16-30 and column 20 lines 41-57));

wherein defining a hierarchical order in the overhead section of digital frame structure communications includes defining an overhead section with a plurality of overhead byte configurations (the FEC value and field size changes over time thus it has multiple configurations (see abstract, column 1 lines 16-30 and column 20 lines 41-57)) and wherein processing communications in response to the hierarchical order of overhead section bytes

includes processing communications in a plurality of processes in response to the plurality of overhead byte configurations (the multiple configurations of the FEC are processed be receiving stations (see abstract, column 1 lines 16-30 and column 20 lines 41-57));

wherein defining a hierarchical order in an overhead section with a plurality of byte locations includes defining a hierarchical order in response to the configuration of overhead byte locations wherein selecting overhead byte locations from the plurality of byte locations includes selecting a first configuration and wherein processing communications in response to the hierarchical order of overhead section bytes includes selecting a first process in response to the first configuration (the FEC value and field size changes over time thus it has multiple configurations and it also in one of a plurality of locations (see abstract, column 1 lines 16-30 and column 20 lines 41-57));

wherein defining a hierarchical order in response to the configuration of overhead byte locations includes defining an overhead section with a plurality of byte locations wherein selecting overhead byte locations from the plurality of byte locations includes selecting a plurality of byte location configurations (the FEC value and field size changes over time thus the cell has multiple configurations where bytes are placed (see abstract, column 1 lines 16-30 and column 20 lines 41-57)) and wherein processing communications in response to the hierarchical order of overhead section bytes includes selecting a plurality of processes in response to the plurality of configurations (inherently, processes must be performed to process the FEC procedures (see abstract, column 1 lines 16-30 and column 20 lines 41-57));

wherein defining a hierarchical order in response to the configuration of overhead byte locations includes defining an overhead section with a first configuration and a second

configuration wherein selecting overhead byte locations from the plurality of byte locations includes selecting a first and a second configuration (the FEC value and field size changes over time thus it has multiple configurations (see abstract, column 1 lines 16-30 and column 20 lines 41-57)) and wherein processing communications in response to the hierarchical order of overhead section bytes includes selecting a first process in response to the first configuration and a second process in response to the second configuration (the FEC changes thus different processes must be used to recognize where in the cell the FEC is and perform the FEC function (see abstract, column 1 lines 16-30 and column 20 lines 41-57));

wherein defining a hierarchical order in an overhead section with a plurality of overhead byte quantities includes defining a hierarchical order in response to configurations of overhead byte quantities (the FEC is determined (see abstract, column 1 lines 16-30 and column 20 lines 41-57)) wherein selecting the overhead byte quantities from the plurality of byte quantities includes selecting a first configuration (the FEC is chosen to be a certain size (see abstract, column 1 lines 16-30 and column 20 lines 41-57)) and wherein processing communications in response to the hierarchical order of overhead section bytes includes selecting a first process in response to the first configuration (inherently, a process is used to perform the FEC (see abstract, column 1 lines 16-30 and column 20 lines 41-57));

wherein defining a hierarchical order includes defining an overhead section with a plurality of configurations of overhead byte quantities (the FEC is configured to be a certain size and value (see abstract, column 1 lines 16-30 and column 20 lines 41-57)) wherein selecting the quantity of overhead bytes from the plurality of byte quantities includes selecting a plurality of configurations (the FEC can vary and thus multiple configurations are selected throughout

communication (see abstract, column 1 lines 16-30 and column 20 lines 41-57)) and wherein processing communications in response to the hierarchical order of overhead section bytes includes selecting a plurality of processes in response to the plurality of configurations (inherently, since the FEC varies a plurality of processes must be used to determine the size, location and values of the FEC (see abstract, column 1 lines 16-30 and column 20 lines 41-57));

wherein defining a hierarchical order in response to configuration of overhead byte quantities includes defining an overhead section with a first configuration and a second configuration (the FEC can be multiple values (see abstract, column 1 lines 16-30 and column 20 lines 41-57)) wherein selecting the quantity of overhead bytes from the plurality of byte quantities includes selecting a first and a second configuration (the FEC is determined and processed while its is a variety of configurations (see abstract, column 1 lines 16-30 and column 20 lines 41-57)) and wherein processing communications in response to the hierarchical order of overhead section bytes includes selecting a first process in response to the first configuration and a second process in response to a second configuration (inherently, processing each FEC has an associated process (see abstract, column 1 lines 16-30 and column 20 lines 41-57));

wherein defining a hierarchical order in an overhead section with a plurality of byte values includes defining a hierarchical order in response to the configuration of overhead byte values wherein selecting overhead byte values from the plurality of byte values includes selecting a first configuration and wherein processing communications in response to the hierarchical order of overhead section bytes includes selecting a first process in response to the first configuration (the FEC value and field size changes over time thus it has multiple configurations (see abstract, column 1 lines 16-30 and column 20 lines 41-57));

wherein defining a hierarchical order in response to the configuration of overhead byte values includes defining an overhead section with a plurality of byte value wherein selecting overhead byte values from the plurality of byte values includes selecting a plurality of byte value configurations (the FEC value and field size changes over time thus it has multiple configurations (see abstract, column 1 lines 16-30 and column 20 lines 41-57)) and wherein processing communications in response to the hierarchical order of overhead section bytes includes selecting a plurality of processes in response to the plurality of configurations (inherently, processes must be performed to process the FEC procedures (see abstract, column 1 lines 16-30 and column 20 lines 41-57));

wherein defining a hierarchical order in response to the configuration of overhead byte values includes defining an overhead section with a first configuration and a second configuration wherein selecting overhead byte values from the plurality of byte values includes selecting a first and a second configuration (the FEC value and field size changes over time thus it has multiple configurations (see abstract, column 1 lines 16-30 and column 20 lines 41-57)) and wherein processing communications in response to the hierarchical order of overhead section bytes includes selecting a first process in response to the first configuration and a second process in response to the second configuration (the FEC changes thus different processes must be used to recognize and perform the FEC function (see abstract, column 1 lines 16-30 and column 20 lines 41-57));

wherein defining a hierarchical order in the overhead section of digital frame structure communications includes selecting a predetermined location in a frame overhead section (the FEC is put into a certain location of the overhead (see figure 23-26 and abstract)) and wherein

processing communications in response the hierarchical order of overhead section bytes includes forward error correcting the overhead bytes in the selected location (the FEC is processed (see abstract, column 1 lines 16-30 and column 20 lines 41-57)).

wherein defining a hierarchical order in the overhead section of digital frame structure communications includes selecting a first location and a second location in a frame overhead section (a first location is for FEC and another location is for an identifier field (VPI/VCI) (see figure 25)) and wherein processing communications in response the hierarchical order of overhead section bytes includes forward error correcting overhead bytes in the first location and not forward error correcting overhead bytes in the second location (the FEC field is for forward error correction and the identifier field (VPI/VCI) is for cell identity and thus not for forward error correction (see figure 25));

receiving the frame with a first error correction value, extracting the overhead bytes in the second location (cells are received that have the FEC in the header and also VPI/VCI values in the header, which are extracted and replaced with updated VPI/VCI values when the user changes its location (see column 6 line 46 through column 7 line 27)) substituting overhead bytes in the second location; and transmitting the frame with the first error correction value (after the new VPI is received from the Home Station it is put in the cell for transport and the FEC is still in the cell (see column 6 line 46 through column 7 line 27));

4. Claims 28-43 are rejected under 35 U.S.C. 102(b) as being anticipated by Pasternak et al. (USPN 5,710,756), hereafter referred to as Pasternak.

Referring to claim 28-43 Pasternak discloses an integrated circuit (IC) relay system for segmenting a digital frame structure, the system comprising at least a first relay node including a frame receiver (an access node of the network (see figure 6)) including an overhead receiver to receive the overhead section of a frame (the node includes an overhead section (see item 65 in figure 6)), a payload receiver to receive the payload section of the frame (the receiver also has a payload receiver (see item 64 in figure 6)), and a decoder to provide a forward error corrected (FEC) frame (the node includes a FEC decoder (see item 67 in figure 6)), wherein the overhead receiver includes an input to select a hierarchical order in the overhead section of received digital lame structure communications (the FEC is part of the overhead and it is selected for the FEC calculation (see figure 6 and column 6 line 53 through column 7 line 15)) and wherein the frame receiver processes communications in response the selected hierarchy (the data cell is processed including the FEC (see figure 6 and column 6 line 53 through column 7 line 67));

wherein the frame receiver processes communications selected from the group including synchronization, scrambling, forward error correction, and node segmented channel communication (the node performs FEC calculations (see figure 6 and column 6 line 53 through column 7 line 67)).

wherein the overhead receiver selects a hierarchy in response to overhead section byte configurations selected from the group including the quantity of overhead bytes, the location of overhead bytes, and the value of overhead bytes (an FEC value is chosen using Reed-Solomon cods (see column 6 line 53 through column 7 line 67));

wherein the overhead receiver selects a hierarchy in response to accepting commands to select overhead byte locations from a plurality of byte locations (the FEC is put into a location of

the overhead out of a plurality of possible overhead locations (see figure 7)) and wherein the frame receiver processes communications in response to the selected overhead byte locations (the FEC is performed (see figure 7));

selecting a quantity of overhead bytes from a plurality of overhead byte quantities and wherein the frame receiver processing communications in response to the selected overhead byte quantity (a certain quantity of overhead is chosen depending upon whether a regular E1 frame is used or an Enhanced E1 frame (see figures 7 and 8));

wherein the overhead receiver selects a hierarchy in response to selecting overhead byte values from a plurality of overhead byte values and wherein the frame receiver processes communications in response to the selected overhead byte values (an FEC value is chosen using Reed-Solomon cods (see column 6 line 53 through column 7 line 67));

wherein the overhead receiver selects a hierarchy in response to selecting a first configuration of overhead bytes and a second configuration of overhead bytes (the cells are transmitted in an E1 frame or and enhanced E1 frame (see figures 7 and 8)) and wherein the frame receiver processes communications in a first process in response to the first configuration, and in a second process in response to the second configuration (the system must inherently perform the appropriate E1 or enhanced E1 processing to transport the frames (see figures 7 and 8));

wherein the overhead receiver selects a hierarchy with a plurality of overhead byte configurations and wherein the frame receiver processing communications in a plurality of processes responsive to the plurality of configurations (the system must inherently perform the appropriate E1 or enhanced E1 processing to transport the frames (see figures 7 and 8));

wherein the overhead receiver selects a hierarchy in response to selecting configurations from a plurality of byte location configurations and wherein the frame receiver processes communications in a plurality of processes responsive to the selected configurations (the ATM cells can be transmitted in E1 frames of enhanced E1 frames thus there are multiple byte location configurations (see figures 7 and 8));

wherein the overhead receiver selects a hierarchy in response to selecting configurations from a plurality of overhead byte quantities and wherein the frame receiver processes communications in a plurality of processes in response to the selected configurations (the ATM cells can travel in E1 or enhanced E1 frames and inherently there are different processed implemented to perform the processing of these different configurations (see figures 7 and 8)).

wherein the overhead receiver selects a hierarchy in response to selecting configurations from a plurality of overhead byte values and wherein the frame receiver processes communications in a plurality of processes in response to the selected configurations (an FEC value is chosen using Reed-Solomon cods (see column 6 line 53 through column 7 line 67)).

wherein the overhead receiver selects a hierarchy in response to selecting a location in a frame overhead section and wherein the frame receiver performs forward error correction of the overhead bytes in the selected location (the node performs FEC calculations (see figure 6 and column 6 line 53 through column 7 line 67));

wherein the overhead receiver selects a hierarchy in response to selecting a location in a frame overhead section, and wherein the frame receiver descrambles the overhead bytes in the selected location (the node also descrambles overhead data (see figure 6 and column 6 line 53 through column 7 line 67));

wherein the overhead receiver accepts commands to select a hierarchy in response to first and second location configurations in the frame overhead section and wherein the frame receiver forward error corrects overhead bytes in the first location, but not in the second location (the frames comprise locations for addressing and FEC, so the FEC location is used for FEC processing and the addressing location is not used for processing (see figures 7 and 8));

at least a second relay node including a frame receiver including an overhead receiver to receive the overhead section of a frame, a payload receiver to receive the payload section of the frame, and a decoder to provide a forward error corrected (FEC) frame, wherein the overhead receiver includes an input to select a hierarchical order in the overhead section of received digital frame structure communications and wherein the first and second relay nodes accept communications including a frame overhead section defining a hierarchy with a first byte location and a second byte location, wherein the first node overhead receiver includes an input to select the first byte location; wherein the first node frame receiver performs a first communication process in response to the bytes in the first location wherein the second node overhead receiver includes an input to select the second byte location and wherein the second node frame receiver performs a second communication process in response to the bytes in the second location (there are a plurality of access nodes having the same parts as the access node in figure 6 and these nodes also process many bytes of the overhead (see figures 1 and 6 and columns 6 and 7));

a first relay node transmitter including a frame generator including an overhead generator to generate the overhead section of a frame, a payload generator to generate the payload section of the frame, and an encoder to provide forward error correction for the frame and wherein the

overhead generator includes an input to select the hierarchical order in the overhead section (the access node includes a payload generator, overhead generator and a FEC decoder (see figure 6)).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 19 and 22-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ayanoglu in view of Tomooka et al (USPN 5,555,477), hereafter referred to as Tomooka.

Referring to claims 19 and 22-24, Ayanoglu discloses the system discussed above. Furthermore, Ayanoglu discloses defining a hierarchical order in the overhead section of digital frame structure communications includes selecting a predetermined location in a frame overhead section (a location in the overhead is chosen for a particular FEC (see abstract, column 1 lines 16-30 and column 20 lines 41-57));

selecting a first location and second location in a frame overhead section (part of the cell overhead includes the FEC and part includes the VPI/VCI values (see abstract, column 1 lines 16-30 and column 20 lines 41-57)).

receiving the frame (the frames are transmitted and received (see figures 2-4)) and reading the overhead bytes in the second location (the VPI/VCI values are read (see figures 2-4));

replacing the overhead bytes in the second location and transmitting the frame with the scrambled overhead bytes in the first location (cells are received that have the FEC in the header and also VPI/VCI values in the header, which are extracted and replaced with updated VPI/VCI values when the user changes its location and after the new VPI is received from the Home Station it is put in the cell for transport and the FEC is still in the cell (see column 6 line 46 through column 7 line 27)).

Ayanoglu does not disclose that processing communications in response the hierarchical order of overhead section bytes includes scrambling the overhead bytes in the selected location. However, Tomooka discloses a system wherein certain bytes of a frame are scrambled (see figure 19). It would have been obvious to one skilled in the art at the time of the invention to implement this feature into the Ayanoglu system because doing so would make the data being transmitted more secure, since scrambling the data provides this benefit.

7. Claims 25-27, as best understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Ayanoglu in view of Nagami et al. (USPN 5,835,710), hereafter referred to as Nagami.

Referring to claims 25-27, Ayanoglu discloses the system discussed above. Ayanoglu does not disclose that different node process different byte locations of the overhead. However, Nagami discloses a system wherein cells are transported across a network wherein certain nodes process ATM values in the header and other nodes process IP (network layer) values in order to transport data. It would have been obvious to one skilled in the art at the time of the invention

to implement this feature into Ayanoglu because doing so would make Ayanoglu operate faster and more efficiently since node all nodes do not have to process *all* of the bytes of the header.

8. Claim 44 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pasternak in view of Nagami.

Referring to claim 44, Pasternak discloses the system discussed above. Furthermore, Pasternak discloses the first node frame receiver receives a frame with a first forward error correction (frames have a first FEC (see figures 7 and 8)) and wherein the second node frame receiver receives the frame with the first forward error correction (the frames are transmitted to other nodes (see figure 1)).

Pasternak does not disclose that the first node frame receiver substitutes overhead bytes in the second location and the first node frame generator transmits a frame with the substituted overhead bytes to the second node receiver. However, Nagami discloses a system wherein cells are transported across a network wherein certain nodes process ATM values in the header and other nodes process IP (network layer) values in order to transport data. It would have been obvious to one skilled in the art at the time of the invention to implement this feature into Ayanoglu because doing so would make Ayanoglu operate faster and more efficiently since node all nodes do not have to process *all* of the bytes of the header.

9. Claims 45 and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pasternak in view of Tomooka.

Referring to claims 45 and 46, Pasternak discloses the system discussed above. Furthermore, Pasternak discloses the first node transmitter has an output connected to the input of the second node receiver (there are many nodes in the network (see figure 1));

Pasternak does not disclose that scrambling the overhead bytes in the selected location. However, Tomooka discloses a system wherein certain bytes of a frame are scrambled (see figure 19). It would have been obvious to one skilled in the art at the time of the invention to implement this feature into the Ayanoglu system because doing so would make the data being transmitted more secure, since scrambling the data provides this benefit.

Conclusion

10. The following prior art, which is made of record and not relied upon, is considered pertinent to applicant's disclosure:

a. U.S. Patent Number 6,675,340 to Hardie et al.

b. U.S. Patent Number 6,657,967 to Fujisawa et al.

c. U.S. Patent Number 6,658,006 to Chen et al.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Odland whose telephone number is (571) 272-3096. The examiner can normally be reached on Monday - Friday from 8am to 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou, can be reached at (571) 272-3088. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

deo

September 4, 2004

HASSAN KIZOU
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600